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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,325	01/09/2004	Masayuki Furumiya	Q79080	7256

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/753,325	FURUMIYA ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 17-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 17-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1, 2 and 8 are objected to because of the following informalities: Claim 1, line 18, the phrase "the diameter" (both occurrences) has no antecedent basis. Claim 2, line 2, the phrase "the same design rule" has no antecedent basis. Claim 8, line 3, the phrase "said third predetermined range" has no antecedent basis. Appropriate correction is required.

2. Claims 1-15 and 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1, lines 10-11, claim 14, lines 9-10, claim 17, lines 9-10, claim 19, lines 9-10, claim 20, lines 9-10, claim 21, lines 9-10, the phrase "a second via that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer" is unclear whether the one wiring layer and the adjacent wiring layer are similar to the one wiring layer and the adjacent wiring layer (lines 7-8 of claims 1, 14, 17, 19, 20, 21) that connect to the first via.

Claim 4, line 2, the phrase "the first via overlap with each other" is vague and indefinite. Claim 1, the parent claim of claim 4, discloses a first via connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer. Fig. 5B further discloses a plurality of via (VA3) formed on a first electrode [2A]. There are no first via overlap with each other.

Claim 4, lines 3-4, the phrase "the second via overlap with each other" is vague and indefinite. Claim 1, the parent claims of claim 4, discloses a second via connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer.

Fig. 4 further discloses a plurality of via (VA3) formed on a first electrode [2B]. There are no second via overlap with each other.

Claim 7, lines 3-4, the phrase "the minimum value of said second predetermined range" is unclear as to what is the boundary of the minimum value.

Claim 8, line 3, the phrase "the minimum value of said third predetermined range" is unclear as to what is the boundary of the minimum value.

Claim 11, lines 3-4, the phrase "the minimum value of said first predetermined range" is unclear as to what is the boundary of the minimum value.

Claim 13, lines 2-3, the phrase "said first and second via are provided in plural numbers the longitudinal direction of said first and second electrodes" is unclear whether it is being referred to "said first and second via are provided in plural numbers in the longitudinal direction of said first and second electrodes".

Claim 20, lines 19-20, the phrase "a region including the region immediately under said first and second electrodes" is unclear whether it is different from the region including the region immediately under said first and second electrodes in lines 16-17 of claim 20.

Claim 21, lines 20-21, the phrase "a region including the region immediately under said first and second electrodes" is unclear whether it is different from the region including the region immediately under said first and second electrodes in lines 17-18 of claim 21.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sowlati et al. (in the IDS filed on 9/21/04) in view of Hajimiri et al. (in the IDS filed on 9/21/04).

In regards to claim 14, Sowlati et al. disclose a semiconductor device in figs. 2A-2C. It comprising: a plurality of wiring layers [22-25] that are laminated with each other, each of said wiring layers comprising: an interlayer insulating film [26-29, 34]; first and second electrodes [22-25] buried in the interlayer insulating film and remote from each other; a first via ([30-32] in layers B) that connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer, and a second via ([30-32] in layers A) that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal B, said connected second electrodes and said second via are connected to a second terminal A, and a capacitor is formed between said first electrodes and said first via connected to said first terminal and said second electrodes and said second via connected to said second terminal; wherein said first and second electrodes are in strip shapes that are parallel to each other; wherein said first and second via are provided in plural numbers in the longitudinal direction of said first and second electrodes.

Sowlati et al. differ from the claimed invention by not showing the distance between said first via in the longitudinal direction of said first electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in

each of said wiring layers, and the distance between said second via in the longitudinal direction of said second electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers.

Hajimiri et al. show the distance between said first via [304] in the longitudinal direction of said first electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers, and the distance between said second via in the longitudinal direction of said second electrode is larger than the distance between the first and second via of said first and second electrodes that are adjacent in each of said wiring layers in fig. 5.

Since both Sowlati et al. and Hajimiri et al. teach a vertical plate capacitor with via, it would have been obvious to have the via arrangement of Hajimiri et al. in Sowlati et al. because they reduce the series resistance of the capacitor.

5. Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida in view of Sowlati et al. (in the IDS filed on 9/21/04).

In regards to claim 17, Yoshida discloses a semiconductor device in fig. 3. It comprising: a first terminal of a capacitor [1] is connected to ground wiring [3] and a second terminal of the capacitor [1] is connected to power source wiring [2].

Yoshida differs from the claimed invention by not showing a semiconductor device comprising: a plurality of wiring layers that are laminated with each other, each of said wiring layers comprising: an interlayer insulating film; first and second electrodes buried in the interlayer insulating film and remote from each other; a first via that connects the

first electrode of one wiring layer to the first electrode of an adjacent wiring layer and a second via that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal, said connected second electrodes and said second via are connected to a second terminal, and a capacitor is formed between said first electrodes and said first via connected to said first terminal and said second electrodes and said second via connected to said second terminal.

Sowlati et al. disclose a semiconductor device in figs. 2A-2C. It comprising: a plurality of wiring layers [22-25] that are laminated with each other, each of said wiring layers comprising: an interlayer insulating film [26-29, 34]; first and second electrodes [22-25] buried in the interlayer insulating film and remote from each other; a first via ([30-32] in layers B) that connects the first electrode of one wiring layer to the first electrode of an adjacent wiring layer, and a second via ([30-32] in layers A) that connects the second electrode of one wiring layer to the second electrode of an adjacent wiring layer, and said connected first electrodes and said first via are connected to a first terminal B, said connected second electrodes and said second via are connected to a second terminal A, and a capacitor is formed between said first electrodes and said first via connected to said first terminal and said second electrodes and said second via connected to said second terminal.

Since both Yoshida and Sowlati et al. disclose a capacitor formed on a semiconductor substrate, it would have been obvious to have the capacitor of Sowlati et al. in Yoshida because it increases the decoupling capacitances of the capacitor.

In regards to claim 18, the combined device further discloses said wiring layers (Sowlati et al.) are formed in a semiconductor chip, and said ground wiring and said power source wiring (Yoshida) are arranged in the periphery of said semiconductor chip.

6. Applicant's arguments filed 6/24/05 have been fully considered but they are not persuasive.

It is urged, in page 14 of the remarks, that it is inappropriate for the Examiner to rely on the Hajimiri because the drawings are not drawn to scale. It is further urged that unless a patent indicates that the drawings are drawn to scale, the proportions of features in a drawing are not evidence of actual proportions (see MPEP § 2125). However, fig. 5 of Hajimiri shows the relative distance between the via in the longitudinal direction of the first or second electrode is larger than the distance between the first and second via of the first and second electrodes that are adjacent in each of the wiring layers. The examiner is not comparing the actual proportions of features in the drawing (the actual dimensions of the via or the electrodes in the drawing) with the actual proportions of features in the claimed invention. The examiner is just comparing the relative proportions of features in the drawing (the distances between the via in two different directions in the drawing) with the relative proportions of features in claimed invention. Therefore, it is believed that the combined device still meets the limitation of the claimed invention.

7. Claims 1 and 19-21 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 8:20 am to 5:50 pm.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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September 2, 2005

Steven Loke
Primary Examiner